

SUB-PATENT Form 1449A/PTO  <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
Application Number				09/933934	
Filing Date				8/20/2001	
First Named Inventor				STEPHEN MELVIN	
Group Art Unit				2662	
Examiner Name				MELVIN MARCELO	
Attorney Docket Number				MIPS.0178-00-US	
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U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
MM		6131163	10-10-2000	Scott L. Wiegel	
MK		6016308	1-18-2000	Crayford et al.	
MM		6502213	12-31-2002	Michel K. Bowman-Amuah	
MM		5408464	04-18-1995	Mark Jurkevich	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> - Number <sup>4</sup> - Kind Code <sup>5</sup> (if known)				

Examiner Signature: <u>Melvin Marcelo</u>	Date Considered: <u>10-28-2005</u>
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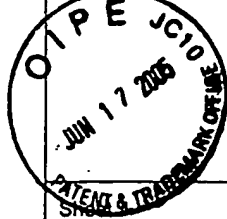
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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number	09/933934
Filing Date	08/20/01
First Named Inventor	Stephen Melvin
Art Unit	2662
Examiner Name	KIZOU, HASSAN
Attorney Docket Number	MIPS.0178-00-US

Sheet	1	of	3
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Examiner Initials*	Cite No.†	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, where Relevant Passages or Relevant Figures Appear
		Number-Kind Code‡ (if known)			
mm		4200927	04-29-1980	Huges et al.	
mm		5708814	1-13-1998	Short et al.	
mm		5724565	03-03-1998	Dubey et al.	
mm		5784649	07-21-1998	Begur et al.	
mm		6460105	10-01-2001	Jones et al.	
mm		6529515	03-04-2003	Raz et al.	
mm		6523109	02-18-2003	Stephan G. Meier	
mm		6640248	10-28-2003	Jacob W. Jorgensen	
mm		6625808	09-23-2003	David R. Tarditi	
mm		6738371	05-18-2004	Lawrence Ayres	
mm		6738378	05-18-2004	Tuck, III et al.	
mm		6813268	11-02-2004	Kalkunte et al.	
mm		6535905	03-18-2003	Kalafatis et al.	
mm		20010004755	06-21-2001	Levy et al.	
mm		20010005253	06-28-2001	Hiroshi Komatsu	
mm		20010052053	12-13-2001	Nemirovsky et al.	
mm		20010043610	11-22-2001	Nemirovsky et al.	
mm		20020016883	02-07-2002	Musoll et al.	
mm		20020049964	04-25-2002	Takayama et al.	
mm		20020083173	06-27-2002	Musoll et al.	
mm		20020071393	06-13-2002	Enric Musoll	
mm		09/608,750	NA	Nemirovsky et al.	
mm		5559970	09-24-1996	Vinod Sharma	
mm		6614796	09-02-2003	Black et al.	

## FOREIGN PATENT DOCUMENTS


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		Country Code* Number*Kind Code‡ (if known)				
MM	AA	WO 03/005645A2	06-25-2002	Sampath et al.		

Examiner Signature	Melvin Marcelo	Date Considered	10-28-2005
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Sheet	2	of	3	

## NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.*	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>†</sup>
MM	BA	MELVIN ET AL., "Extended Instruction Set for a Packet Processing Applications," July 5, 2001, Disclosure Document #496559, USPTO	
MM	BB	MUSOLL ET AL., "Hardware Algorithm for Allocating and De-Allocating Consecutive Blocks of Memory," April 3, 2001, Disclosure Document #491557, USPTO	
MM	BC	MUSOLL ET AL., "Mechanism to Overflow Packets to a Software Controlled Memory When They Do Not Fit into a Hardware Controlled Memory," July 3, 2001, Disclosure Document #496391, USPTO	
MM	BD	MUSOLL ET AL., "Mechanism to Activate a Context When No Stream is Running in a Multi-Streaming Processing Core," April 16, 2001, Disclosure Document #492431, USPTO	
MM	BE	MUSOLL, ENRIC, "Functional Validation of a Packet Management Unit," May 18, 2001, Disclosure Document #429011, USPTO	
MM	BF	SAMPATH ET AL., "Mechanism to Un-speculatively Pre-fetch Instructions from the Thread Associated to a Packet," April 2, 2001, Disclosure Document #491527, USPTO	
MM	BG	YAMAMOTO, WAYNE. An Analysis of Multistreamed, Superscalar Processor Architectures. University of California Santa Barbara Dissertation. December 1995. Santa Barbara, US.	
MM	BH	YAMAMOTO ET AL. "Increasing Superscalar Performance Through Multistreaming." Parallel Architectures and Compilation Techniques (PACT '95). 1995	
MM	BI	The PowerPC Architecture: A Specification for a New Family of RISC Processors. 2 <sup>nd</sup> Ed. May 1994. pp. 70-72. Morgan Kaufmann. San Francisco, US.	
MM	BJ	MC68020 32-Bit Microprocessor User's Manual. 3 <sup>rd</sup> Ed.. 1989. pp. 3-125, 3-126, and 3-127. Prentice Hall, NJ, US.	
MM	BK	POTEL, M. J. "Real-Time Playback in Animation Systems." Proceedings of the 4 <sup>th</sup> Annual Conference on Computer Graphics and Interactive Techniques. 1977. pp. 72-77. San Jose, CA, US.	
MM	BL	ARM Architecture Reference Manual. 1996. pp. 3-41, 3-42, 3-43, 3-67, and 3-68. Prentice Hall, NJ, US.	
MM	BM	MUSOLL ET AL. Mechanism to Prevent the Download of a Packet with Pending Writes Affecting Its Data. April 11, 2001. Disclosure Document #492430, USPTO	
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mm	BN	ESA/390 Principles of Operation. IBM Online Publications Center Reference Number SA22-7201-08. Table of Contents and paras. 7.5.31 and 7.5.70. IBM Corporation. Boulder, CO, US.	
mm	BO	MC88110 Second Generation RISC Microprocessor User's Manual. 1991. pp. 10-66, 10-67, and 10-71. Motorola, Inc.	
mm	BP	DIEFENDORFF ET AL. "Organization of the Motorola 88110 Superscalar RISC Microprocessor." IEEE Journal of Microelectronics. April 1992. pp. 40-63. Vol. 12, No. 2. IEEE. New York, NY, US.	
mm	BQ	KANE, GERRY. PA-RISC 2.0 Architecture. 1996, pp. 7-106 and 7-107. Prentice Hall. NJ, US.	
mm	BR	DIEFENDORFF ET AL. "AltiVec Extension to PowerPC Accelerates Media Processing." IEEE Journal of Microelectronics. Vol. 20, No. 2 (2000): pp. 85-95	
mm	BS	GRUNEWALD ET AL. "Towards Extremely Fast Context Switching in a Block Multithreaded Processor." Proceedings of EUROMICRO 22, 1996. pp. 592-599	
mm	BT	BRADFORD ET AL. "Efficient Synchronization for Multithreaded Processors." Workshop on Multithreaded Execution, Architecture, and Compilation. Jan-Feb 1998. pp. 1-4	
mm	BU	PAI ET AL. "An Evaluation of Memory Consistency Models for Shared-Memory Systems with ILP Processors." Proceedings of ASPLOS-VII, Oct. 1996: pp. 12-23, ACM, Inc.	
mm	BV	YOAZ ET AL. "Speculation Techniques for Improving Load Related Instruction Scheduling." 1999. Pages 42-53, IEEE.	
mm	BW	KESSLER, R. E. "The Alpha 21264 Microprocessor: Out-of-Order Execution at 600 MHz." August 1998.	
mm	BX	DONALSON ET AL. "DISC: Dynamic Instruction Stream Computer, An Evaluation of Performance." 26th Hawaii Conference on Systems Sciences. Vol. 1. 1993. Pages 448-456.	
mm	BY	NEMIROVSKY ET AL. "DISC: Dynamic Instruction Stream Computer." ACM. 1991. Pages 163-171	
mm	BZ	UNGERER ET AL. A Survey of Processors with Explicit Multithreading. ACM Computing Surveys, Vol., 35, No. 1. March 2003. Pages 29-63.	
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